IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TELCORDIA TECHNOLOGIES, INC., Plaintiff/Counterclaim Defendant, v. LUCENT TECHNOLOGIES, INC., Defendant/Counterclaim Plaintiff.	)	C.A. No. 04-875-GMS
	)	**REDACTED PUBLIC VERSION**
TELCORDIA TECHNOLOGIES, INC., Plaintiff/Counterclaim Defendant, v. CISCO SYSTEMS, INC., Defendant/Counterclaim Plaintiff.	)	Civil Action No. 04-876-GMS

VOLUME 2 OF 2 OF EXHIBITS TO TELCORDIA TECHNOLOGIES, INC.'S AUGUST 25, 2006 LETTER TO JUDGE SLEET IN RESPONSE TO THE DEFENDANTS' REQUESTS FOR LEAVE TO FILE SUMMARY JUDGMENT MOTIONS

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Dated: September 1, 2006

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United States Patent [19]

Chao et al.

[11] **Patent Number: 4,893,306**

[45] **Date of Patent: Jan. 9, 1990**

[54] **METHOD AND APPARATUS FOR MULTIPLEXING CIRCUIT AND PACKET TRAFFIC**

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[21] Appl. No.: **118,977**

[22] Filed: **Nov. 10, 1987**

[51] Int. Cl.[4] H04J 3/16; H04J 3/26

[52] U.S. Cl. 370/94.2; 370/84; 370/99; 370/112

[58] Field of Search 370/94, 60, 84, 99, 370/111, 112, 82, 110.1, 89

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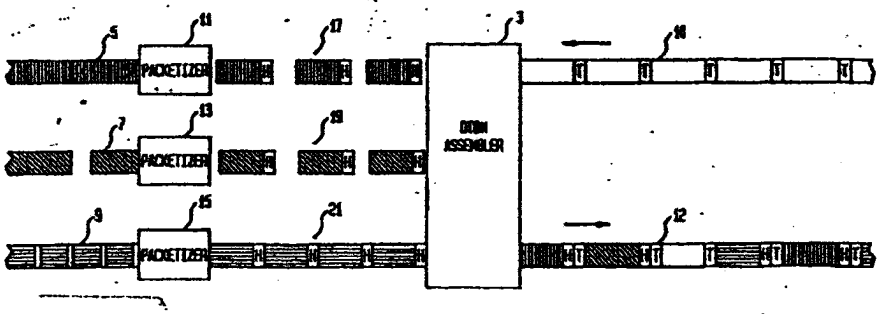
[57] **ABSTRACT**

A data transmission technique referred to herein as Dynamic Time Division Multiplexing (DTDM) is disclosed along with a set of multiplexers and demultiplexers required to apply DTDM in an actual telecommunications network. The DTDM technique uses a transmission format which is compatible with the existing digital circuit transmission format and the packet transmission format so that DTDM is able to handle the transmission of circuit and packet traffic. Thus, DTDM provides a flexible migration strategy between present circuit networks and future broadband packet networks.

7 Claims, 10 Drawing Sheets



parallel-to-serial converter 216 and serial output 206 so as to define a train of empty DTDM frames. Other information comprising the transmission overhead (T) field of the DTDM frame may also be stored in ROM 234 or provided by other sources connected to the bus 219 via a tristate device operative under the control of the control unit 219.

In particular situations (see e.g., framers 70 of FIG. 5 and 126 of FIG. 9), a framer unit receives occupied DTDM frames and the header (H) or transmission overhead (T) fields have to be examined to control peripheral circuit operations such as the reading of data into a FIFO. In this case, a multiple byte delay unit 230 may be included in the path between the serial input 202 and the parallel and serial outputs 208, 206. Typically a frame arrives at the serial input 202 and is converted to parallel form by the serial-to-parallel converter 212. The frame detector detects the frame and supplies necessary information from the header or transmission overhead fields to the control unit 210 which issues appropriate control signals via lines 232 such as user read/write strobes. Illustratively, the user read/write strobes control the writing of data from DTDM frames in the framer unit into associated FIFOs or other buffers. If the FIFO has byte wide format, the parallel output 206 may be used for this purpose. The delay unit 230 is used to insure that the necessary signal processing takes place before the DTDM frame leaves the framer unit.

7. Conclusion

A data transmission technique known as Dynamic Time Division Multiplexing (DTDM) has been disclosed along with an end-to-end network utilizing DTDM.

Finally, the above described embodiments of the invention are intended to be illustrative only. Numerous alternative embodiments may be devised by those skilled in the art without departing from the spirit and scope of the following claims.

What is claimed is:

1. A method for simultaneously transmitting data from sources having different bit rates in a telecommunication network comprising the steps of:

generating a bit stream comprising a sequence of frames, each of said frames including a transmission overhead field containing frame timing information and an empty payload field, and

filling the empty payload fields in said frames with data in packetized format from a plurality of sources which have access to the bit stream including circuit or packet sources, such that data in packetized format from any of said sources is written into any available empty payload field of any of said frames for transmitting data from each of said sources at its own desired bit rate via said bit stream and for transmitting data from said plurality of sources simultaneously via said bit stream.

2. The method of claim 1 wherein prior to filling said frames with slots from a circuit transmission stream, said slots are converted to said packetized format by placing a header in front of each of said slots.

3. A method for generating a bit stream capable of transporting data originating from both circuit transmission and packet sources comprising

generating a bit stream comprising a sequence of frames, each of said frames including a transmission overhead field containing frame timing information and an empty payload field,

packetizing data from a plurality of sources having different bit rates and which have access to said bit stream including circuit transmission sources or customer premises equipment to produce data packets, and

inserting said packets from said sources into the empty payload fields of said frames such that a packet from any of said sources is inserted into any available empty payload field of any of said frames for transmitting data from each of said sources at its own desired bit rate via said bit stream and for transmitting data from said plurality of sources simultaneously using said bit stream.

4. An apparatus for assembling a dynamic time division multiplexing bit stream comprising,

generating means for generating a train of frames wherein each frame includes a transmission overhead field containing timing information and an empty payload field,

processing means for processing data from a plurality of sources into packet format, and

inserting means for receiving said train of frames and for inserting each of said packets comprised of data from one of said plurality of sources into any empty payload field of any of said frames available to said inserting means to form said bit stream so that data from each of said sources can be transmitted at its own desired bit rate via said bit stream and so that data from said plurality of sources can be transmitted simultaneously via said bit stream.

5. The apparatus of claim 4 wherein said sources include circuit transmission bit streams or customer premises equipment.

6. An apparatus for assembling a bit stream for transmitting data from a plurality of sources comprising:

means for generating a train of frames, each of said frames including a transmission overhead field and an empty payload field, and

a plurality of interfaces, each of said interfaces serving to interface one of said sources with said train of frames, each of said interfaces comprising:

packetizing means for converting data into data packets,

memory means for storing at least one of said packets formed by said packetizing means, and

circuit means for inserting a packet stored in said memory means into any empty payload field of any available one of said frames so that data from each one of said sources can be transmitted at its own desired bit rate via said bit stream and so that data from said plurality of sources can be transmitted simultaneously via said bit stream.

7. The apparatus of claim 6 wherein said interface units are connected to one another serially and wherein said frames are passed sequentially to each of said interface units to receive said packets in said empty payload fields.

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Synchronous Techniques for Timing Recovery in BISDN

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Globecom '92

ABSTRACT

The issue of timing recovery for an ATM network is inherently different from its circuit-switched counterpart. There are generally two classes of approaches: non-synchronous methods rely on cell jitter filtering while synchronous methods use common reference clock. The latter approach has better jitter/wander performance. This is particularly significant for circuit emulation of existing hierarchical signals (e.g. DSn signals), which have stringent jitter/wander requirements. This paper compares several different methods for timing recovery in synchronous network environment. The fundamental concept, implementation, and performance of three synchronous techniques: Synchronous Frequency Encoding Technique (SFET), Time Stamp (TS), and Synchronous Residual Time Stamp (SRTS), are discussed. Among these methods, it is concluded that the SRTS method is the most efficient. In addition, it is observed that a strong analogy can be drawn between SRTS and conventional pulse stuffing synchronization techniques. Based on the analogy, it is shown that the jitter performance for SRTS is comparable to that of the circuit-switched network.

1. Introduction

Asynchronous Transfer Mode (ATM) is a packet oriented technology for the realization of Broadband Integrated Services Network (BISDN). By using ATM, network resources can be shared among multiple users. Moreover, various services including voice, video and data can be multiplexed, switched, and transported together under a universal format. Full integration will likely result in simpler and more efficient network and service administration and management. However, while conventional circuit-switching is optimized for real-time, continuous traffic, ATM is more suitable for the transport of bursty traffic such as data. Accommodation of constant bit rate (CBR) services is, however, an important feature of ATM, both for universal integration and for compatibility between existing and future networks.

The transport of a CBR signal through a broadband ATM network is usually referred to as circuit emulation. One of the critical issues of circuit emulation concerns the recovery of the source clock frequency at the receiver. This is the topic studied in this paper. Timing recovery for ATM circuit emulation is quite different from the conventional timing recovery problem since in the conventional circuit-switched network, a constant bit rate service such as a DS1 is usually synchronized to the network timing via pulse stuffing techniques.

In an ATM network, the CBR service is first segmented into 47-octet units and then mapped, along with an octet of ATM Adaptation Layer (AAL) overhead, into the 48-octet payload of the cell. The cells are then statistically multiplexed into the network and routed through the network via ATM switches. Due to the statistical multiplexing of cells at the source and the queuing delays incurred at the ATM cell switches, the periodicity of the real time circuit-switched signal is destroyed. As a result, the cells carrying the circuit-switched service do not arrive at the destination node periodically. The deviation from the ideal arrival times (in units of time) is called "cell jitter". Cell jitter is difficult to filter out for two reasons: the amplitude of the cell jitter can be large compared to the service cell period, and the statistics of the cell jitter are generally unknown, other than the fact that the average is zero.

2. Desired Criteria for Timing Recovery

Before we discuss different timing recovery approaches, we would like to look at some criteria for their evaluation. In the list below, the first item is most important, especially for circuit emulation of existing signal such as a DS1, since performance requirements for existing signals already exist. Other items are considered to be desirable guidelines and are listed in order of decreasing significance.

- Jitter/Wander performance: For circuit emulation such as carrying existing North American hierarchical signals (e.g. DS1, DS3), jitter performance is very important. CCITT recommendations on the control of jitter and wander specifies that the jitter on a DS1 signal should not be larger than 1.5 Unit Intervals (U.I.) at 10 Hz. More stringent requirements are stated for higher frequency jitter. G.824 also specifies an 18μsec requirement for wander at very low frequency (<< 1Hz). Jitter control of a DS1 signal is important to assure proper timing recovery at a DS1 terminal. The control of wander is necessary to reduce the slip rate when the signal is terminated at a DS0 switch. If, however, the CBR signal terminates at a customer premise equipment (CPE), the requirement for wander might be relaxed.
- Flexibility to accommodate different bit rates: A desired timing recovery feature is the ability to be used for different service rates. A generalization of this feature is the ability to accommodate even timing information that has no direct relationship to the service bit rate (e.g. video sampling rate in compressed video transmission).
- Implementation complexity: An example is to implement a Phased-Locked Loop (PLL) with very low cutoff frequency (a few Hz). This requires special design and is considered to be more complex than a commercially available PLL with higher cutoff frequencies (e.g. 100 Hz).
- Protocol simplicity: If transmitter information is needed, a simple protocol for carrying this information is desirable.
- Robustness to transmission errors and cell losses: A good timing recovery system should be robust to transmission errors (both random and burst errors) and cell losses/misinserts. In general, detected cell losses should not upset the recovered timing.
- Convergence time: It is desirable to have fast convergence time to reduce buffer size and, therefore, the associated delay.

S_n is then known within the magnitude of residual error (5.1) that

$$[M_{min} + d_n] \le S_n \le [M_{max} + d_n] \quad (5.3)$$

Since the maximum and minimum of d_n are 1 and 0 respectively, S_n is bounded by,

$$[M_{min}] \le S_n \le [M_{max}] + 1 \quad (5.4)$$

This implies, that the most significant portion of S_n carries no information and only the least significant portion needs to be transmitted. This is the basic idea of RTS. The minimum resolution required to represent the residual part of S_n unambiguously is a function of N, the ratio of the network derived frequency to the service frequency, and the service clock tolerance, $\pm\varepsilon$. The maximum deviation, y, between M_{nom} and the maximum or minimum values of M (M_{max} or M_{min}) is given by,

$$y = N \times \frac{f_{ne}}{f_s} \times \varepsilon \quad (5.5)$$

As an example consider the case where f_{ne} = 155.52 MHz and f_s = 78.16 MHz (nominal) and an RTS sampling period is 3008, corresponding to 8 cells and a 47-octet SAR_PDU per cell. For this example, M_{nom} = 5985.2119. If we further assume that the source clock tolerance is 200 parts per million, i. e., $\pm 200\times10^{-6}$, it follows from (5.5) that y = 1.197. This clearly demonstrates that it is superfluous to transmit the full S_n in each RTS sampling period and transmission of the last few (P) bits of S_n is sufficient. This P-bit sample is the Residual-TS (RTS). The generation of the RTS in the transmitter is shown in Figure 5. In this circuit, counter C_T is a P-bit counter which is continuously clocked by the network derived clock. The output of counter C_T is sampled every T seconds (N service clock cycles).

Consider the previous example and assume that a four-bit counter (P=4) is used. Since M_{nom} = 5985.2119 = 1.2119 (Modulo 16), a typical RTS output sequence will look as follows;

$$\ldots,5,6,7,9,10,11,12,13,15,1,2,\ldots \quad (5.6)$$

Since the counter, in effect, quantizes by truncation, the RTS changes only by integer values. The changes in RTS are such that their average is exactly equal M_{nom} (modulo 2^P). In the example, the changes are either 1 or 2 with the change of 2 occurring either every 4 or 5 RTSs in such a way that the average interval is 1/0.2119 = 4.7198. In general, successive RTSs are related by

$$RTS_{n+1} = RTS_n + S_n = RTS_n + [d_n + M_n] \ (modulo\ 2^P) \quad (5.7)$$

where P is the number of bits in the counter. To guarantee that no information is lost due to the modulo arithmetic, i.e., that the transmitted RTS represent S_n unambiguously, it is seen from (5.4) that the number of bits used for transmission must satisfy:

$$2^P \ge [M_{max}] - [M_{min}] + 2 \quad (5.8)$$

Thus, in the example given, the number of bits allocated to the RTS must be 3 or greater.

If (5.8) is satisfied, knowledge of M_{nom} in the receiver along with the received RTSs may be used to reproduce the source clock from the synchronous network clock. Many implementations are possible. In the one shown in Figure 6, the received RTSs are first stored in an RTS FIFO which is used to absorb the network cell jitter. The RTSs from the FIFO are then compared to a free-running P-bit counter, driven by the (synchronous) network derived clock (f_{ne}), that may be thought of as a receiver RTS generator. The phase locked loop acts to keep this RTS generator in synchronism with the transmitted RTSs. Whenever the output of Counter C_R matches the current RTS, the comparator generates a pulse. Since Counter C_R is modulo 2^P, the comparator output consists of a train of pulses (see Figure 7). Except for the first pulse, these are 2^P cycles apart. In order to pick out the correct pulse, gating circuitry (inside the dotted box) is used. The timing diagram in Figure 7 shows the operation of the gating circuitry. The circuit generates a gating pulse after M_1 cycles. M_1 is given by,

$$M_1 = [M_{nom}] - 2^{(P-1)} \quad (5.9)$$

This will ensure that $[M_{max}] - 2^P < M_1 < [M_{min}]$, thus the gating pulse is guaranteed to select the correct RTS. The output of the gating circuit, i. e., the proper C_R pulse, is then used as the reference signal for the PLL as well as the reset for the gating circuit.

5.1 Choice of RTS Parameters and its Transport

The relations between the RTS sampling period, the clock frequency ratios, service clock tolerance, and size of the RTS have already been discussed. Based on such considerations, the following parameters were chosen in the December 1991 CCITT meeting [12].

- N=3008, (8 cells)
- $\frac{f_{ne}}{f_s} \le 2$
- Tolerance accommodated: $\le 200\times10^{-6}$
- Size of RTS: 4 bits

The choice of N and the 4-bit RTS is based on the framing structure inherent in the 3-bit sequence number that was also specified in CCITT. The 4-bit RTS can be transmitted in the serial bit stream provided by the CSI bit in the SAR sublayer, with the 3-bit sequence number providing a frame structure over 8 bits in this serial channel. Four bits of the framed 8 bits are allocated for the RTS while the remaining 4 bits are used for the indication of a CS pointer [12]. A frequency ratio of less than 2 was specified since it is more than adequate to satisfy jitter requirements and so that the 4-bit channel could robustly accommodate the RTS. The network derived clock (f_{ne}) can easily be generated from the 155.52 MHz network clock (f_n). Service rates ranging from 64 Kb/s to the full capacity of the STS-3c payload can be accommodated if

$$f_{ne} = 155.52\,MHz \times 2^{-k}, \qquad k=0,1,\ldots 11 \quad (5.10)$$

Since the SAR overhead is already protected by a 3 bit CRC and a parity bit, no added protection for transmission error was deemed necessary. The RTS is inherently robust enough to cope with cell loss. Since the maximum uncertainty of M is 1.2, four consecutive RTSs could be lost and the correct M still determined from the 4-bit RTS.

5.2 Analogy with pulse stuffing techniques

It is interesting to note that the SRTS method has a strong analogy with conventional positive/negative pulse stuffing techniques. This analogy allows jitter analysis based on existing results. In a conventional positive stuffing system, the stuffing opportunities come every M_c+1 bits (M_c is an integer) so that the number of bits of data transmitted is either M_c+1 or M_c (see Figure 8). A nominal stuffing ratio of ρ means that positive

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Trans Comm Soc
June '93
Preprint

Synchronous Techniques for Timing Recovery in BISDN

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Abstract - **Timing recovery for an ATM network is inherently different from its circuit-switched counterpart. There are two generic approaches to ATM timing recovery, namely, non-synchronous methods which rely on cell jitter filtering and synchronous methods which use a common reference clock. The latter approach has better jitter/wander performance. This is particularly significant for circuit emulation of existing hierarchical signals (e.g. DSn signals), which have stringent jitter/wander requirements. This paper compares several methods for timing recovery in a synchronous network environment and discusses the fundamental concept, implementation, and performance of three synchronous techniques: Synchronous Frequency Encoding Technique (SFET), Time Stamp (TS), and Synchronous Residual Time Stamp (SRTS). Among these methods, it is concluded that the SRTS method, invented by the authors, is the most efficient. SRTS has been accepted by ITU-T as the timing recovery standard for AAL-1 (ATM Adaptation Layer - Circuit Emulation). Practical implementation considerations of the SRTS technique and its robustness against cell loss are also examined in this paper. In addition, it is shown that a strong analogy can be drawn between SRTS and conventional pulse stuffing synchronization techniques so that the jitter performance for SRTS is comparable to that of the circuit-switched network.**

I. Introduction

Asynchronous Transfer Mode (ATM) is a packet oriented technology for the realization of Broadband Integrated Services Network (BISDN). By using ATM, various services including voice, video and data can be multiplexed, switched, and transported together in a universal format thus permitting network resources to be shared among multiple users. The full integration of various services may also allow simpler and more efficient network and service administration and management. The transport of a constant bit rate (CBR) signal through a broadband ATM network is usually referred to as circuit emulation. Accommodation of CBR services is an important feature of ATM both for universal integration and for compatibility between existing and future networks, even though ATM is more suitable for the transport of bursty traffic such as data. One of the critical issues of circuit emulation, the recovery of the source clock frequency at the receiver, is the topic studied in this paper. The technique proposed here [16] has been adapted by ITU-T (formerly CCITT) as the standard for timing recovery for the ATM Adaptation Layer - type 1.

The timing recovery problem for ATM circuit emulation is quite different from the conventional one. In the conventional circuit-switched network, a constant bit rate service such as DS1 is synchronized to the network timing via pulse stuffing techniques. These have been studied extensively [1]. Implementation usually involves a phase-locked loop (PLL) to smooth the gapped clock that is produced when the stuffed pulses and other network overhead are removed from the network clock. Conventional timing recovery techniques, however, cannot be directly applied to circuit emulation in an ATM network. The basic transport and switching entity of ATM is a fixed-size *cell*. The ITU-T standard [2] for an ATM cell has 53 octets. Five octets are assigned to be the header which contains information for link-to-link routing, priority indication, forward error correction as well as cell-type identification. The cell header is terminated at an ATM switch which performs link-to-link routing. Above the ATM layer is the adaptation layer. Currently, 5 types of AAL are defined for applications including CBR services, video, and data. The adaptation overhead for CBR services is called AAL type 1. It contains one overhead octet which supports end-to-end functions including timing recovery and cell loss detection, leaving 47 octets for the transport of user information. To transport a CBR service through the ATM network, the CBR service's bit stream is first segmented into 47-octet units and then mapped along with the AAL byte into the ATM cells. The assembled cells are then statistically multiplexed into the network and routed through the network via ATM switches. Due to the statistical multiplexing of cells at the source and the queuing delays incurred at the ATM cell switches, the periodicity of the real time circuit-switched signal is destroyed and, as a result, the cells carrying the circuit-switched service arrive at the destination node aperiodically. The deviation from the ideal arrival times is called "cell jitter". Such cell jitter is difficult to filter out for two reasons. First, the amplitude of the cell jitter is large compared to the period of the source clock, and, second, the statistics of the cell jitter are generally unknown except that the its average is zero.

A number of timing recovery methods have been studied in the literature. In order to compare these methods, we first examine desirable criteria and requirements in Section 2. We will describe briefly two non-synchronous timing recovery techniques in Section 3. Synchronous methods, the main

Paper approved by Gerard P. O'Reilly, the Editor for Communications Switching of the IEEE Communications Society.
Manuscript received: September 19, 1993; revised: February 15, 1994
Conference Information: This paper was presented in part at Globecom, Orlando, Florida, December 1992.
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knowledge of the received RTS and M_{min}. A reference signal (s_r) with pulses that are S_n units of network derived clock apart can then be generated and used to drive a PLL which performs a multiply-by-N function as well as a filtering function for the jitter.

Many implementations for the recovery of S_n are possible. In Fig. 7(a), we show an implementation which does not require elaborate computation. The basic idea is to duplicate the generation of the RTS at the receiver. Let us first assume that the circuit is initialized, i.e. the PLL is synchronized to the received RTS, the gating pulse is just reset, and a new RTS is output from the RTS FIFO. This RTS is compared to a free-running P-bit counter C_R, which is driven by the (synchronous) network derived clock (f_{nx}). Each time the output of counter C_R matches the current RTS, the comparator generates a pulse. Since Counter C_R is modulo 2^P, the comparator output consists of a train of pulses as shown in Fig. 7(c). Except for the first pulse immediately after the reset, these pulses are 2^P cycles apart. From (5.7), we know that one of these pulses will give us the correct S_n. We also know, as a result of (5.4) and (5.8), that the correct RTS pulse will occur during the interval between $[M_{min}]$ and $[M_{min}]+2^P-1$ inclusive, as illustrated in Fig. 7(b). Thus, if we look at a window starting just before $[M_{min}]$, and stopping just after $[M_{min}]+2^P-1$, we will encounter only one RTS pulse, which corresponds to S_n. This selection mechanism is provided by a gating signal which is generated by the circuitry within the dotted-line box in Fig. 7(a). The output of the gating circuit, i. e., the correct RTS pulse, is then used as the reference signal for the PLL. The reference pulses, which are exactly S_n units apart, are also used to reset the gating circuit and read out the next RTS. The functions of the PLL include the generation of N clock cycles between the consecutive reference signal pulse and the filtering of the phase variation resulting from the quantization of M_n. As will be shown below, a simple off-the-shelf PLL is sufficient for satisfying the jitter requirements.

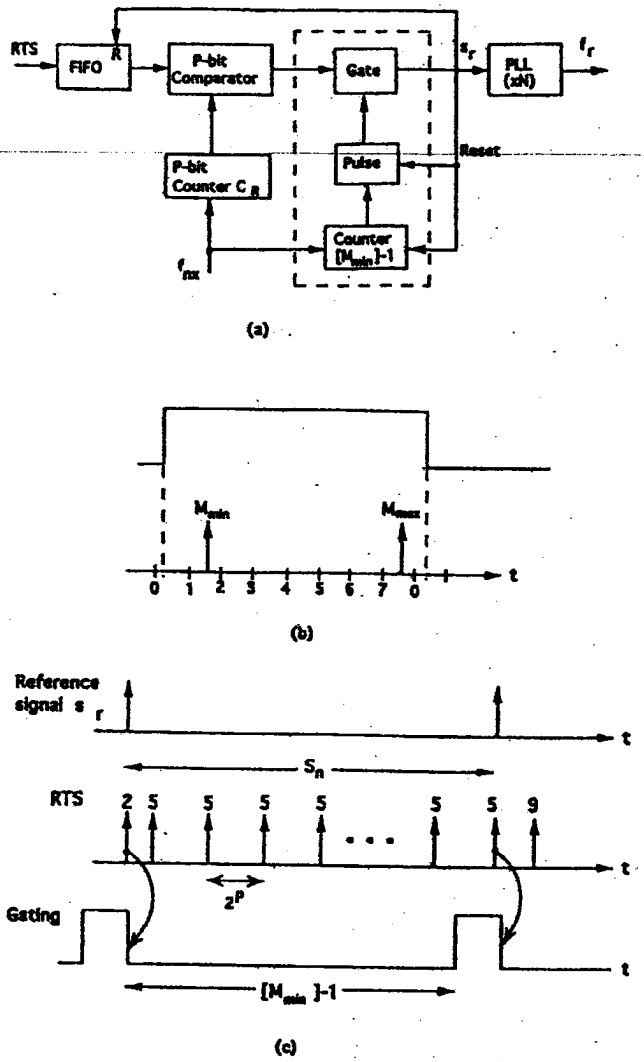

Fig. 7. The SRTS receiver: (a) reconstruction of the source clock; (b) example showing possible range of RTS (assuming $P = 3$); (c) timing diagram showing the gating function

C. CHOICE OF RTS PARAMETERS AND TRANSPORT

The relations between the RTS sampling period, the clock frequency ratios, source clock tolerance, and size of the RTS have already been discussed. Based on such considerations, CCITT [2] chose N=3008 (8 cells), $1 \le r = \frac{f_{nx}}{f_s} < 2$, source clock tolerance of 200 ppm, and a 4-bit RTS. The choice of N is based on the framing structure inherent in the 3-bit sequence number that was also specified by CCITT. Keeping the ratio of the frequencies of the network derived clock and the source clock within a factor of two represents a tradeoff between jitter performance and the number of bits required to represent the RTS. If the ratio (r) is too low, a unit of interval (U.I.) of the network derived clock corresponds to many U.I. of the source clock. This means that y as given in (5.5) would be very small. However, the resulting jitter performance would suffer since a peak-to-peak jitter amplitude of 1 U.I. of the network derived clock converts to many U.I. of the recovered clock. On the other hand, if the ratio is too high, implying that f_{nx} is much faster than f_s, more bits would be required to represent the RTS. Moreover, the hardware would have to be operated at a higher rate than the source clock. To satisfy the requirement of r <2 for applications with different rates, a family of network derived clock (f_{nx}) can easily be generated from the 155.52 MHz network clock (f_n). Service rates ranging from 64 Kb/s to the full capacity of the STS-3c payload can be accommodated if

$$f_{nx} = 155.52\,MHz \times 2^{-k}, \quad k=0,1,\ldots 11 \qquad (5.9)$$

With N chosen as 3008, r <2, and the tolerance of 200 ppm, the minimum number of bits to represent the RTS is 3. As we will show below, the choice of a 4-bit RTS provides more robustness against consecutive loss of RTSs. The 4-bit RTS can be transmitted in the serial bit stream provided by the CSI bit in the SAR sublayer, with the 3-bit sequence number of

EXHIBIT 68

REDACTED

EXHIBIT 69

REDACTED

EXHIBIT 70

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EXHIBIT 71

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EXHIBIT 72

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EXHIBIT 73

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EXHIBIT 74

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EXHIBIT 75

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EXHIBIT 76

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EXHIBIT 77

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EXHIBIT 78

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EXHIBIT 79

REDACTED

EXHIBIT 80

REDACTED

EXHIBIT 81

REDACTED

EXHIBIT 82

REDACTED

EXHIBIT 83

REDACTED

CERTIFICATE OF SERVICE

I hereby certify that on the 1st day of September, 2006, the attached **REDACTED PUBLIC VERSION OF VOLUME 2 OF 2 OF EXHIBITS TO TELCORDIA TECHNOLOGIES, INC.'S AUGUST 25, 2006 LETTER TO JUDGE SLEET IN RESPONSE TO THE DEFENDANTS' REQUESTS FOR LEAVE TO FILE SUMMARY JUDGMENT MOTIONS** was served upon the below-named counsel of record at the address and in the manner indicated:

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